REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. §1.116.

Claims 1-20 are pending in this application. In this response, Claims 1 and 9 have been amended. Specifically, Applicants have amended Claim 1 to recite a varactor structure including a semiconductor substrate that includes a subcollector of a second conductivity type located below an upper region of the semiconductor substrate and a semiconductor layer of a first conductivity type beneath the subcollector, in which the first conductivity type is different from said second conductivity. Support for this amendment can be found throughout the originally filed application. More specifically, paragraph 0073 describes that in one embodiment the varactor 22 includes a p-type polysilicon gate conductor 26, an underlying P-well region 20B, adjacent N-well regions 20A and 20C that are separated from the varactor by isolation regions 16, and an underlying n+ subcollector 14 which isolates the P-well region 20B from the body, i.e, semiconductor layer beneath the n+ subcollector 14, of the p-type semiconductor substrate 12. Applicants have also made similar amendments to Claim 9.

Further search is not required for consideration of amended Claims 1 and 9 as the limitations added are components of the semiconductor substrate and therefore previous searches relating to the semiconductor substrate are applicable to amended Claims 1 and 9. Since the above amendments do not introduce any new matter into the application entry thereof is respectfully requested. Turning to the present grounds of rejection.

Claims 1-3, 6-9 and 12-14 are rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent Application Publication No. 2003/0122128 to Coolbaugh et al. ("Coolbaugh et al."). Applicants traverse the aforementioned rejection and submit the following.

It is axiomatic that anticipation under §102 requires the prior art reference to disclose every element to which it is applied. *In re King,* 801 F.2d 1324, 1326, 231 USPQ 36, 138 (Fed Cir, 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: absence from the applied reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that Coolbaugh et al. fails to anticipate Applicants' invention, because the applied prior art reference fails to disclose each and every limitation of Applicants' claimed structure, as recited in amended Claims 1 and 9. More specifically, Coolbaugh et al. fails to disclose a varactor structure including a semiconductor substrate that includes a subcollector of a second conductivity type located below an upper region of the semiconductor substrate and *a semiconductor layer of a first conductivity type beneath the subcollector*, in which the first conductivity type is different from said second conductivity, as recited in amended Claim 1. Amended Claim 9 includes similar limitations as amended Claim 1.

Applicants observe that there is no disclosure of a semiconductor layer beneath the subcollector 12 of the device disclosed in Coolbaugh et al. Referring to Figure 10 of Coolbaugh et al., as cited by the Examiner, the subcollector 12 is clearly depicted as being the lowermost layer of the structure, therefore failing to disclose a semiconductor layer of a first conductivity

type beneath the subcollector, as recited in amended Claim 1. Further, Coolbaugh et al. fails to disclose a varactor structure comprising a p-type semiconductor substrate including an n-type subcollector located below an upper region of the semiconductor substrate and a *p-type semiconductor layer* beneath the n-type subcollector, as recited in amended Claim 9. Therefore, Applicants submit that Coolbaugh et al. fails to disclose each and every element of the claimed invention and respectfully request withdrawal of the rejection under 35 U.S.C. §102(b).

In light of the above, Applicants respectfully submit that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the number listed below.

Respectfully submitted,

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